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Volume 5

iRel40

Intelligent Reliability 4.0

Newsletter M36

"Intelligent Reliability 4.0" (iRel40) is a project with the ultimate goal of improving reliability of electronic components and systems by reducing failure rates along the entire value chain.

Welcome to this fifth newsletter of the ECSEL JU project "Intelligent Reliability 4.0 (iRel40)". The target of iRel40 is to enhance the reliability of electronic components and systems along the value chain from wafer to chip, package/board and system throughout the whole lifecycle in the domains transport and smart mobility, energy and digital industry. The project is in the final stage and many results are already achieved, strengthening development and production of devices with improved reliability considering the value chain from chip to application. Thus, iRel40 supports the sustainable success of investment in microelectronics in Europe through the improvements of the reliability of electronic systems.

This newsletter at month M36, a half year before the project end, provides the status of eleven selected innovations from nine use cases and two test vehicles, which are single technology bricks. All these eleven technical contributions support at least one of the five objectives of iRel40 to improve reliability. We start with five examples from chip technology, followed by three examples from package and package/board technology, continue with one example from testing and close with two examples related to applications.

Inside this issue

Facts & Figures

Partners: 75
Countries: 13
Budget: 101.8 Mio €
JU Funding: 24.5 Mio €
National funding 22.9 Mio €
Project Start: May 1st, 2020
Duration: 42 months
Coordinator: Infineon Technolo-

Newsletter introduction

In addition to the eleven innovations, the results from 4 deliverables in work package WP2 as examples of achieved outcomes are reported. These four deliverables present results from applying computer science including machine learning algorithms, artificial intelligence, and digital twin technologies, as well as compact modelling and combination of physics of failure and data driven models to microelectronics reliability. They are a basic for a high number of new results generated in the iRel40 project.

Intensive collaboration within the consortium was supported by the third General Assembly meeting in Crete, which allowed face-to-face discussions of iRel40 partners about the most critical issues regarding reliability within the project. More than 100 publications based on journal and conference articles were published or are under preparation including a book on iRel40 outcome. The strong iRel40 participation on EuroSimE 2023 conference with 9 contributions in Graz is summarised at the end of the newsletter. During this conference Julia Zündel from AT&S received a best poster award for her contribution on "Influence of the quality of material models on warpage and lifetime prediction by finite element simulation".

iRel40 project consortium

Large enterprises

R&D institutes

Small and medium sized enterprises

iRel40 project objectives

Objective 1
Define needs and requirements for future ECS applications to drive improvements and prediction of reliability along the value chain, chip, package, board/system – to foster Europe's competitiveness in ECS.

Objective 2
Implement data value chains and cross-component data analytics to speed up the learning curves.

Objective 3
Double the predicted lifetime for specific materials and load conditions for ECS applications.

Objective 4
Early detection of unexpected quality relevant events along the ECS value chain by advanced and innovative control concepts.

Objective 5
Reduce the failure rates and enable lifetime prediction with connected and new concepts along the ECS value chain.

#1. Conditional burn-in (IP-6)

(Use case example, Objectives no. 2, 4, 5)

In Industrial Pilot IP-6, we propose a new concept to reduce 100% burn-in (BI) and still fulfill the quality target $\pi_{target} \in [0,1]$ for early life failures. To this aim, we infer a lot-specific health indicator *h* on basis of production data available from different sources, see Fig. 1.1. The health information provided by *h* is merged with the health information obtained from the BI study and, further, related via regression with the early life failure probability *p* of production lots. Finally, a novel Clopper-Pearson-like interval estimator for *p* is introduced.

In the previous months, we have successfully verified the overall concept based on simulated data. Currently, we evaluate the feasibility of IP-6 on further data. Moreover, a scientific paper illustrating the novel approach is in preparation.

Considering real data, the health indicator *h* is a latent variable that has to be estimated. For this task we developed and applied various AI models in the past. Recently, based on the learnings experienced from these models, the available models have been refined and some additional models have been introduced. As of now, the following models are available:

- A Long Short Term Memory (LSTM) autoencoder and a binary classifier trained on logistic and production control data,
- A probabilistic support vector regression (PSVR) and a deep neural network (DNN) trained on data from electrical product tests, and
- A convolutional autoencoder combined with a support vector machine trained on wafer-map test data.

Each of these models has been proven to correlate with the early life failure probability *p* and, thus, provide valuable health information of individual production steps. In the next steps, we investigate to combine the health information provided by the individual AI models to one overall health indicator.

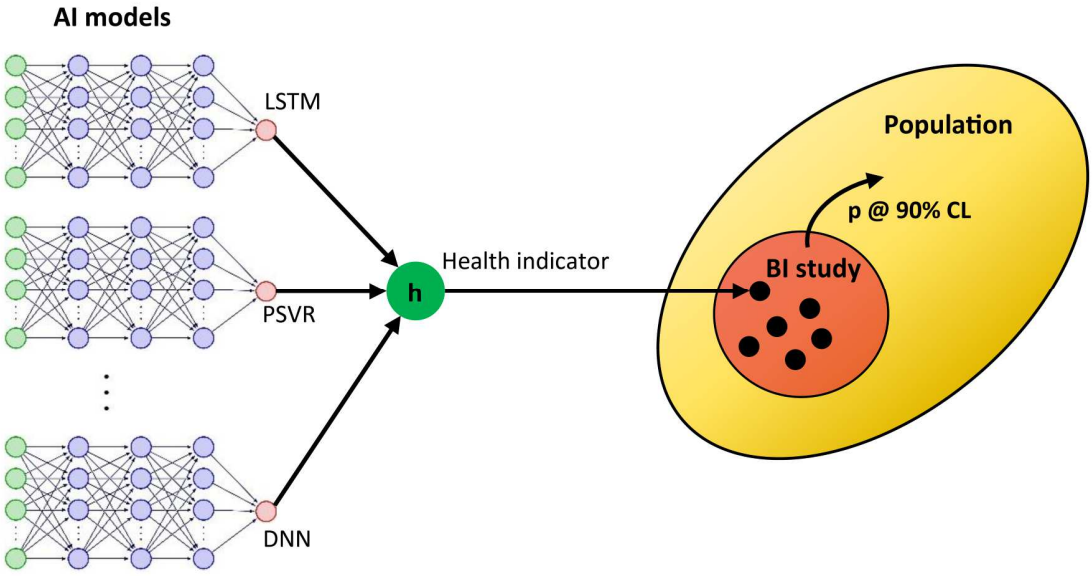

Fig. 1.1: Concept for lot-specific BI.

SELECTED TECHNICAL INNOVATIONS

#2. Automated classification of semiconductor defect density SEM images using deep learning (IP-2)

(Use case example, Objectives no. 1, 2, 4, 5)

The early detection of defect density issues in semiconductor production is crucial for product reliability because it prevents failures of the final product. To assure reliability, numerous inspections are performed. One of them is an inspection by a *Scanning Electron Microscope (SEM)* generating high-resolution images of defects on wafers (see Fig. 2.1). Defect classification is currently performed manually by experts. The goal of this project was to automate the defect image classification with a *Deep Learning (DL)* pipeline. The heart of this DL pipeline is a convolutional neural network (CNN) model. The basis to train such models are historical images stored in the production database. We exported two datasets with images of different complexity and applied data preparation methods to them to create our training datasets. The less complex dataset, called *Carinthia* dataset, contains few classes of defect images of only one technology and one inspection layer. The complex dataset, called *Madrid* dataset, contains a multitude of classes of defect images of different technologies and inspection layers.

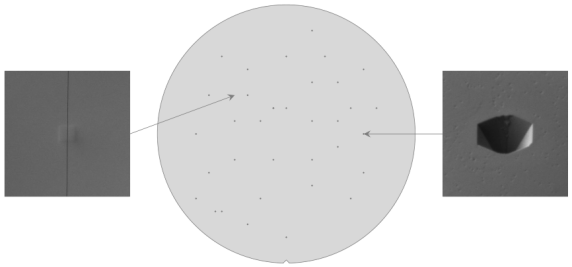

Fig. 2.1: SEM image examples of detected defects.

Both datasets are highly imbalanced. Therefore, we applied data balancing methods prior to model training. We performed and evaluated model-centric experiments on the less complex *Carinthia* dataset and data-centric experiments on the complex *Madrid* dataset. For the model-centric approach, we kept the *Carinthia* dataset and the data balancing method fixed and trained and tuned the following state-of-the-art CNN models: *InceptionV3*, *ResNet50* and the *EfficientNet-B0* (see Fig. 2.2). *ResNet50* slightly outperforms the other two models with an F1-score of 99% on the test dataset. For the data-centric approach on the *Madrid* dataset, we selected the *EfficientNet-B1* model, fixed the hyperparameters and conducted experiments with different data balancing methods in a first step and iteratively improved the quality of the dataset by collecting more data in the second step. The final model, trained on a resampled and augmented *Madrid* dataset, has an F1-score of 94% on the validation dataset. Both models are deployed in production and a regular mode performance check is installed. In case of discrepancies, new data will be collected and the model re-trained.

For future work, we see promising opportunities to further improve the performance of the *Madrid* model by evaluating different CNN architectures and applying hyperparameter tuning. Furthermore, the model monitoring and model update concept can be advanced to reach a higher degree of automation. Other focus could be the automatic detection of new defect classes, which is referred to as novelty detection or open-set recognition in literature.

CNN model	Learning rate	Batch size	F1-score	Validation loss
Inception V3	10^{-1}	2	0.992	0.091
ResNet50	10^{-2}	9	0.994	0.030
EfficientNet-B0	10^{-1}	9	0.990	0.045

The SGD optimizer and the CCE loss function were used for all models.

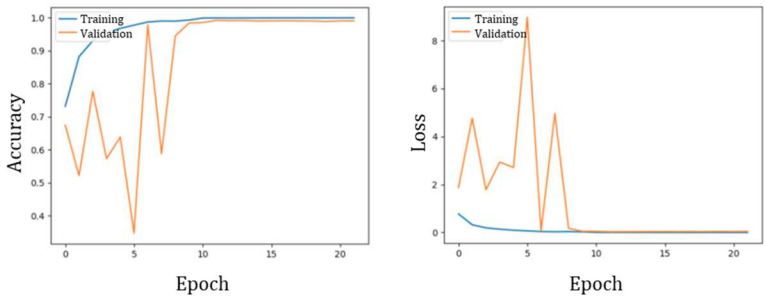

Fig. 2.2: Results for the model-centric experiments on the Carinthia dataset and the training plots of the best model, the ResNet50.

SELECTED TECHNICAL INNOVATIONS

#3. High performance SiC temperature sensor in a CMOS technology for extreme temperature measurement (IP-3)

(Use case example, Objectives no. 1, 2, 4)

The demand for sensors in harsh-environment is growing rapidly as they can be applied in a wide range of industrial applications, for instance, health monitoring of power modules. The traditional harsh environment sensing systems are usually equipped with bulky cooling units and involve putting control electronics in the cooler environment. However, this requires more wiring and longer wiring runs, which causes extra reliability problems. Therefore, there is an urgent need for sensors that are integratable with high-temperature compatible electronics.

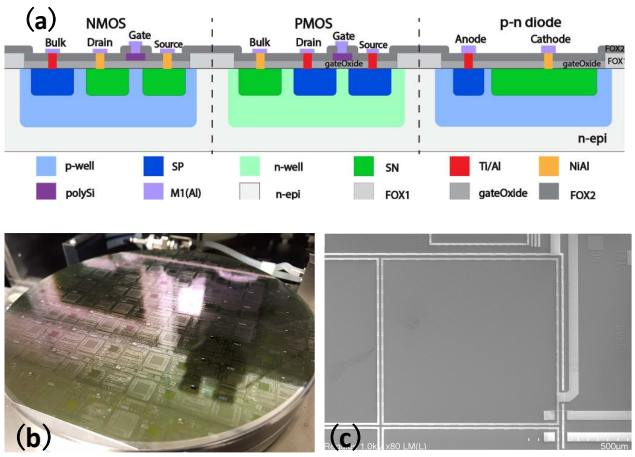

Fig. 3.1: (a) The layer composition of FhG IISB's SiC CMOS technology; (b) A 6-inch SiC wafer containing SiC circuits and sensors; (c) An SEM iamge of the measured SiC temp. sensor.

Within the iRel40 project, a silicon carbide (SiC) CMOS (complementary metal-oxide-semiconductor) technology is developed by Fraunhofer IISB, targeting producing integrated circuits (ICs) in challenging environments. The advantage of SiC over Si is that SiC has around 3 times larger bandgap than Si does, providing a much higher operating temperature for the SiC electronics. The schematic overview of the cross-section and a as-fabricated 6-inch SiC wafers are demonstrated in Fig.3.1a and 3.1b. Like any other mature silicon (Si) IC technology, temperature sensors can also be fabricated with existing doping layers or deposited layers in this CMOS technology. In this project, the SiC p-n diode is characterized for high-temperature sensing from room temperature up to 600°C.

The fabricated device shows diode behavior at all the measured temperature (Fig. 3.2a). The measurement result shows that the SiC temperature sensor has an almost perfect linear voltage output with respect to temperature (Fig. 3.2b). The maximum coefficient of determination (R^2) obtained is 99.98%, and the maximum sensitivity to temperature is 3.04 mV/°C. Fig. 3.2c reveals that the sensor has good output reproducibility under multiple thermal cycles. This sensor can be directly integrated with SiC CMOS readout electronics via the metal layer provided in the technology, forming a monolithically SiC smart sensor. As shown in Fig. 3.2d, the chip is attached to the ceramic glass sample provided by BSH to showcase the potential application in temperature measurement on the inductive cooktop.

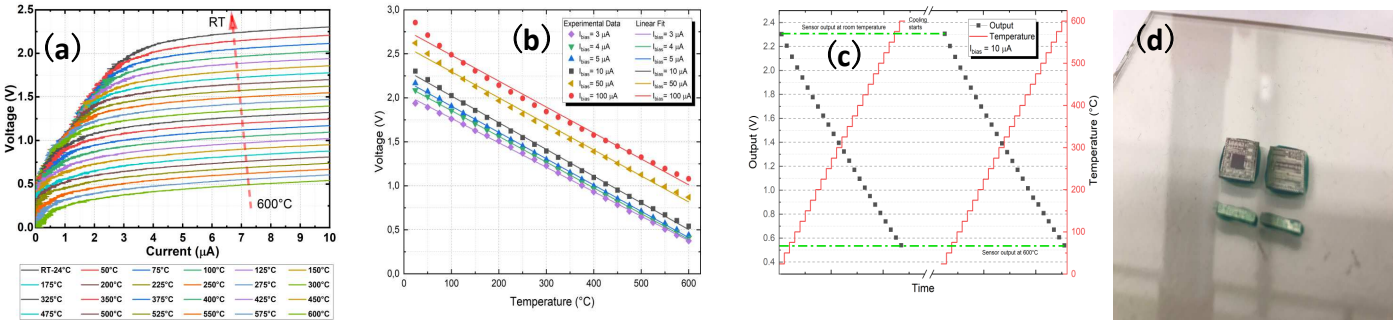

Fig. 3.2: (a) I-V curve of the SiC diode from room temperature up to 600°C; (b) The temperature reponse of the sensor under different bias current levels; (c) Repeatability test; (d) Attaching the sensor to ceramic glass (IP-3).

SELECTED TECHNICAL INNOVATIONS

#4. Novel method for physical characterization of nanometer-sized defects in GaN HEMT devices

(Test vehicle example, target objective no. 4)

Normally-on GaN HEMTs are of great importance for RF and power applications like DC-DC conversion rectifiers, wireless power, LiDAR, satellite communication, base stations for mobile services and radar. The lifetime of GaN devices is limited by irreversible changes in the HEMT structure which decrease the electrical performance up to breakdown. One failure mode is an increased gate leakage current under operating and increased voltage and temperature stress conditions, which could be caused by structural degradation mechanisms like pit formation at gate edges, diffusion of gate metals to the Schottky interface and material losses in the AlGaN barrier. Often the increase in gate leakage current corresponds to the number and/or the intensity of electroluminescence (EL) spots, which can be used to localize potential structural defects at the gate. But due to the limitation of the optical resolution there is a high risk of removing nm-sized inhomogeneities at the HEMT structure during preparation for the following physical analysis. Within the iRel40 project Fraunhofer IMWS developed a novel strategy combining large area planar and additional cross-sectional preparation to pinpoint nm-sized defects in relation to these EL spots making them accessible for high resolution electron microscopy analysis. The analysis workflow was successfully applied for normally-on GaN HEMT devices provided by UMS. The University of Padua performed electrical stressing of the devices until increased leakage at the Schottky gates could be observed. To initiate electrical active degradation these devices were stressed up to significant changes in the electrical performance and then Electroluminescence spots were detected identifying possible defect positions. Metal intrusions into the AlGaN/GaN stack underneath the Schottky gate contacts of only 20nm size could be identified as root cause for the electrical leakage. Analytical TEM investigations of the defects reveal Pt and Au inside the semiconductor reaching the 2DEG at a threading dislocation of the HEMT, thus contributing to the gate leakage current and causing the increased leakage current after electrical testing.

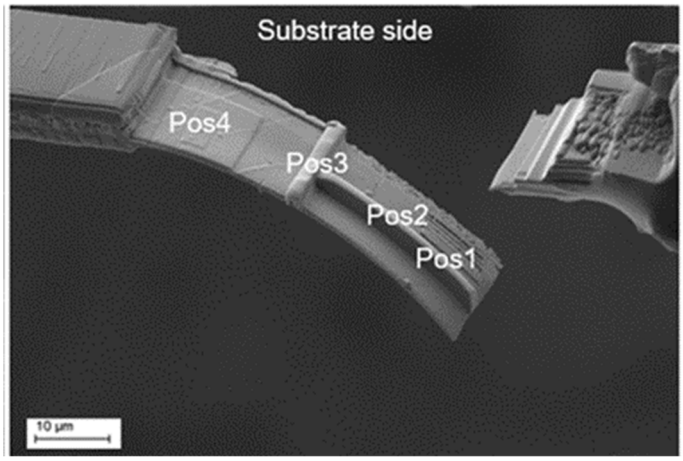

Fig. 4.1: FIB-Preparation of additional cross- sectional electron transparent lamellas at located defect sites out of a planar TEM sample of a degraded HEMT structure reduction.

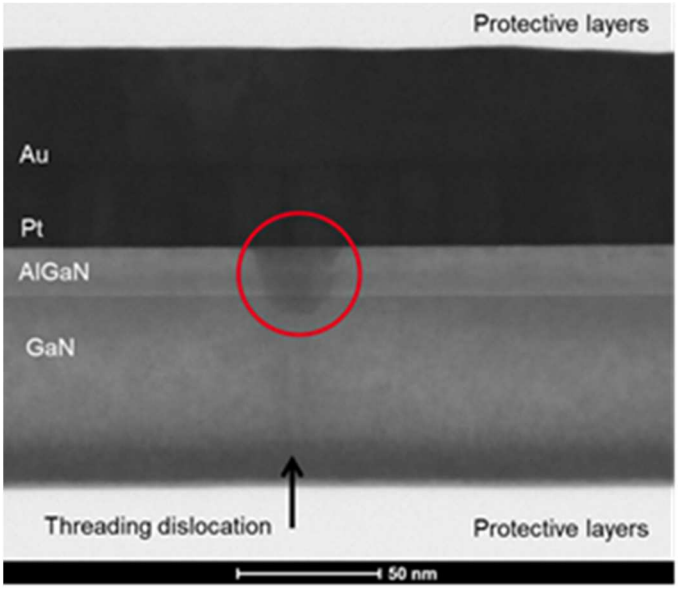

Fig. 4.2: High resolution transparent electron microscopy image of nm sized metal intrusions within the active AlGaN/GaN layers

Fraunhofer IISB

#5. Enabling SiC MOSFET operation at 500°C via a Pt based CMOS compatible metallization

(Test vehicle example, target objectives no. 1, 4)

With silicon reaching its operation limit for temperatures beyond 200°C, special solutions are required. One solution is the usage of higher bandgap semiconductors, such as silicon carbide (SiC). Going towards 500°C and beyond, conventional Al-based metallization starts to degenerate, opening reliability issues even for short operation time. Thus, a change of material is necessary. Therefore, Fraunhofer IISB developed a SiC CMOS compatible high temperature Pt module to address this temperature range.

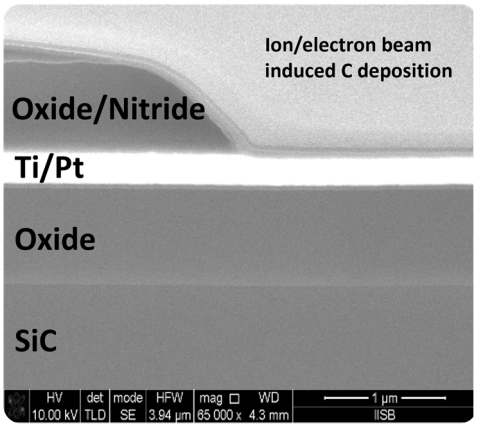

Fig. 5.1: FIB prepared SEM cross section view of a contact pad with Ti/Pt metallization and patterned oxide nitride passivation.

Pt is known for its temperature stability and chemical inertness, making it a promising material choice. Due to the complex topography and various different interfaces in the CMOS technology, an adhesion layer, in this case Ti, is essential to prevent detachment of the metal layer. For patterning the Pt, a lift-off process is applied. Finally, a patterned and dry etched nitride oxide stack passivates the surface, protecting it against environmental influence. A SEM cross section view of the high temperature compatible layer stack is depicted in Fig. 5.1.

First MOSFET samples have been fabricated using IISB's 4H-SiC 2 µm double-well CMOS process including the above mentioned high temperature layers stack. This technology is also available to customers in its early access prototype form via EUROPRACTICE IC service (*https://europractice-ic.com/technologies/asics/fraunhofer-iisb/*), making it unique within Europe. Electrical characterization of NMOS and PMOS devices was performed at IISB including I-V transfer and output characteristics. Investigated temperatures range from room temperature up to 550°C. Fig. 5.2 displays the transfer & output characteristics of a NMOS 20-6, meaning 20 µm channel width and 6 µm channel length, and a PMOS 80-6 up to 550°C, thus proving functionality at high temperatures. The next process run along with further optimization with respect to met-

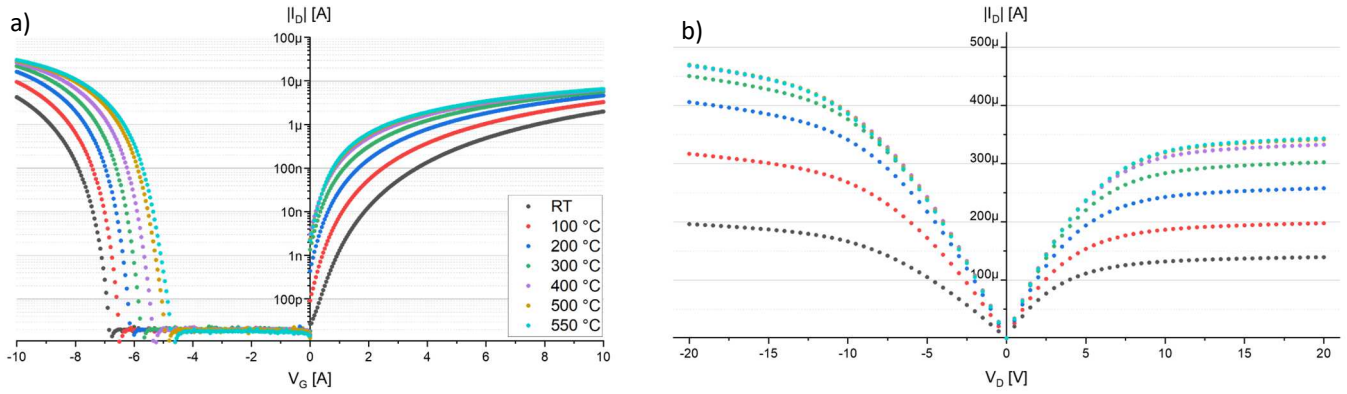

Fig. 5.2: a) Transfer and b) output characteristics of a NMOS 20-6 (at positive voltages) and a PMOS 80-6 (at negative voltages) up to 550°C. Both MOSFETs were fabricated using IISB's HT CMOS technology.

al layer thickness and passivation thickness and choice of materials is currently in fabrication. Additionally, diffusion barriers could significantly improve long term reliability and are therefore currently being evaluated. Nevertheless, successful high temperature operation has been demonstrated.

SELECTED TECHNICAL INNOVATIONS

#6. Modelling & simulation: solder ball reliability simulation comparing cyclic hardening & Anand material models (IP-11)

(Use case example, Objectives no. 1, 2, 4, 5)

Solder ball cracking is a common failure mechanism that often occurs during thermal cyclic reliability testing of assembled printed circuit boards (PCBA). Within the scope of iRel40, simulations were performed using a PCBA model already well-established at AT&S with the aim to understand the main differences of solder ball material models including either cyclic hardening or a visco-plastic material law.

Table1: Investigated models.

Simulation Models	*Step*	*Time [second]*
Global model	Static non-linear	Not dependent
Submodel-1	Static non-linear	Not dependent
Submodel-2	Visco plastic	4800 [s] per cycle
Submodel-3	Visco plastic	9600 [s] per cycle
Submodel-4	Visco plastic	2400 [s] per cycle

The lifetime of solder balls has been rated by comparing different scenarios based on those material laws. Plastic equivalent strain (PEEQ) and cumulative equivalent plastic strain (CEEQ) of different material laws from literature were compared. PEEQ is calculated based on the total deformation and is used to determine the onset of yielding in material accumulated plastic strain. CEEQ is calculated based on the cumulative deformation and is used to capture the damage accumulation and final failure of a material. In order to calculate PEEQ and CEEQ of a solder ball, the whole PCBA (global model) was simulated first, heating from -55°C to +125°C and cooling down to -55°C again. The displacements from the global model are used as boundary conditions for the local model, a so-called submodel of the solder ball modelled in detail. Four different submodels have been studied; all models are summarized in Table 1. Taking a closer look to Fig. 6.1, differences in accumulated strain at the last cycle are visible. In contrast, the position of the strain maxima is always the same. Comparing the data of Submodel-3 and Submodel-4 to Submodel-1 and Submodel-2, the importance and power of the Anand model is visible (Fig. 6.2). The time-effect can easily be addressed by the law and the impact can be studied. The reliability can be improved by adaption of the temperature and time profile. The Anand model can provide answers to such engineering questions easily, since the parameters are well studied in the literature. The cyclic hardening material can only account for the testing speed used during its characterization and implementation. Thus, literature data is not that commonly available and an Anand model is in general recommended for solder fatigue studies.

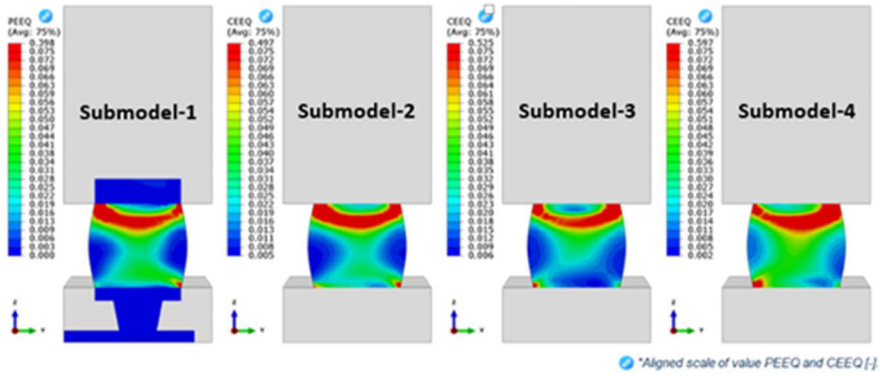

Fig. 6.1: Cumulative equivalent plastic strain (CEEQ) and plastic equivalent strain (PEEQ), deformation scale factor 1.

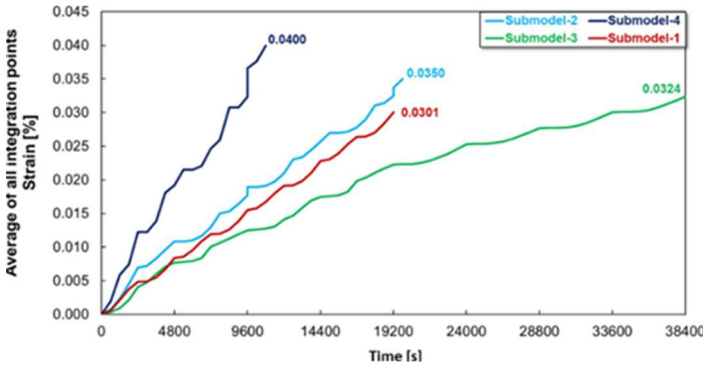

Fig. 6.2: Simulation results of each submodel.

SELECTED TECHNICAL INNOVATIONS

#7. Universal approach for using a stress sensing sytem for package development and reliability testing (T-9)

(Use case example, Objectives no. 2, 4, 5)

Within the iRel40 project in one of the 34 Use Cases stress measurement chips (SMCs) were applied to TO263 packages to investigate reliability behavior of materials. The focus was set on fastening and improving the measurement method toward standardization.

A fast method using an SMC in-situ measurements on Printed Circuit Boards (PCBs) was developed. Seventeen SMC were soldered to PCBs and underwent in-situ measurements during 1000 temperature cycles TC (-55°C/150°C). The test boards were mounted on a mainboard and connected to a manual multiplexer to control the measurement from chip to chip during live measurement in the temperature cycling oven (see Fig. 7.1). Samples were provided by IFAG, the experiment with further improvement of the read-out software was performed at Fraunhofer ENAS. A web-based evaluation software called "SMZ-Analyzer" was developed

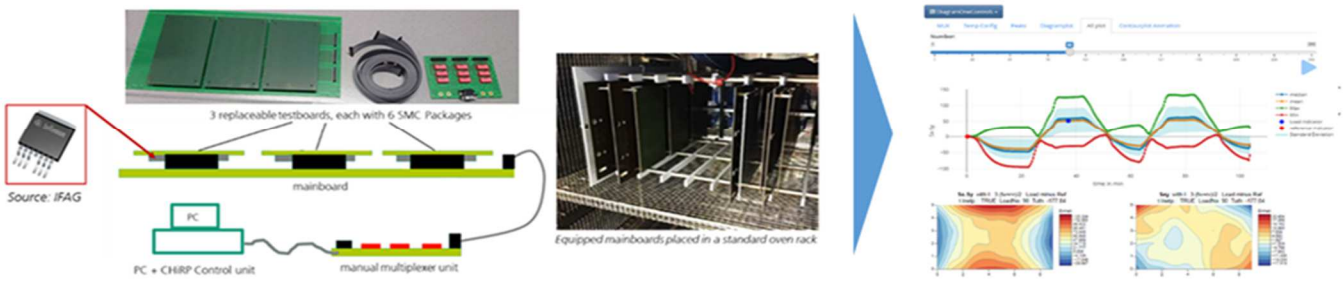

Fig. 7.1: Schematic overview of the manufactured test devices (testboards, mainboard, multiplexer unit) for universal read-out approach and post-processing toll for data analysis „SMC Analyzer".

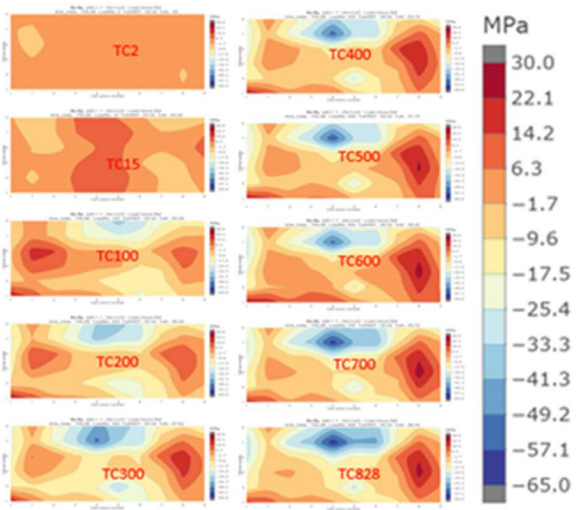

Fig. 7.2: Difference stress (σD) on the chip surface at different time intervals during TC (-55°C/150°C) at -55°C.

using programming language R for fast and easy analysis of SMC data, including visualization.

In this study, the stress level on the surface of the SMC was assessed at various time points during a temperature cycling (TC) experiment conducted at -55°C and 150°C. The measurements were also taken at room temperature at different time intervals for the packages comprising four different molding compound materials. A substantial amount of data, consisting of 140,000 data points obtained from in-situ chip measurements, was gathered from a single SMC-demonstrator. The stress level evaluation at -55°C during the TC experiment of the demonstator is shown in Fig. 7.2.

The integration of SMC measurements with a quick and efficient post-processing application offers a holistic approach for measuring, evaluating, and analyzing the stress levels of SMCs during reliability experiments. The combination with simulation can further enhance the analysis and interpretation of measurement results, enabling identification of failure modes, which can be explored in future investigations. This measurement method can also be utilized to validate simulation models, thereby improving virtual prototyping capabilities and fastening product development.

SELECTED TECHNICAL INNOVATIONS

#8. Smart digital twin testing environment for digital hardware (IP-1)

(Use case example, Objectives no. 1, 2, 4, 5)

The engineering process of electronic components involves various stages, starting from defining the requirements to managing the evidence for certification. To ensure the quality of this process the engineers require the intelligent support of tools that can extract information from requirements industry standards and help to automatically build smart testing environments by generating test cases and testing components at the same time. In this manner, the engineering process is assisted by tools and techniques during the whole V model lifecycle, building a smart layer of capabilities on top of existing tools as an intelligent supervisor for engineering electronic components.

With these needs in mind, nowadays the extraction of requirements information, the generation of test cases and the management of evidences are done manually. The engineers must study the system requirements and other artifacts, such as design components to understand the information and generate test cases and test environments by hand. This process is very costly and can cause errors in the reliability assessment due to the lack of total system coverage. At the same time, evidence management is not carried out automatically, which complicates the verification and validation processes of the system.

Within the iRel40 project it is proposed to develop a system focused on the improvement of the engineering process of electronic components. To do so, it is based on guiding the whole engineering process using intelligent techniques that take the reliability and safety requirements as inputs, providing support to engineers from the inception of the product (smart authoring) to the Verification and validation process (smart testing environment). In this manner, it is possible to save costs and time in the whole engineering process, detecting errors earlier in the system lifecycle, keeping consistency and high quality by default and paving the way towards zero failure.

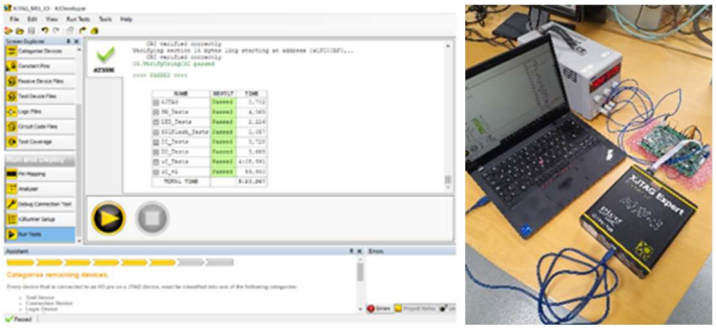

Fig. 8.1: System set-up in real environment.

Through a collaborative work of ULMA, providing the use case and offering development support (Fig. 8.1), the REUSE Company developing functionality and improving its tools and the UC3M university with a focus on research, it has been developed a system for the automatic generation of test cases (Fig. 8.2) and extraction of requirements information and evidence management through a smart digital twin tool (Fig. 8.3).

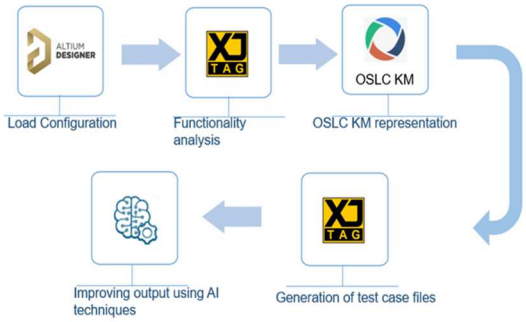

Fig. 8.2: Process for automatic generation of test cases.

Fig. 8.3: Process for evidence management with the smart digital twin.

#9. Smart partial discharge diagnostics for prognostics & health management of electrical and electronic power devices (E-1)

(Use case example, Objectives no. 4, 5)

The increasing power (both voltage and current) of power electronics (PE) with lower losses and costs, enhances the employability for electric power (EP) supply. High voltage (HV) equipment and PE share that electric fields can be ≳ 3 kV/mm. Similar failure modes then occur in EP and PE equipment. One is electric breakdown of deteriorated insulation, preceded by partial discharges (PD) which may have been triggered by transients. PD is sparking in voids, insulation interfaces and at sharp conductor edges. Continued PD erodes the insulation leading to full breakdown. A blessing in disguise: PD pulses may be detected as failure precursors.

IWO develops smart maintenance, weighing Prognostics and Health Management (PHM) technology to prevent unforeseen EP and PE component and system failure and allow timely maintenance actions. Forecasting is indispensable. Digital twins were developed for various types of failure (teething, early wear, random and wear) and maintenance strategies (corrective (CM), period based (PBM) and condition based (CBM)). Though CM, PBM and CBM can all benefit from the smart revolution, CBM is most explicit with diagnostics based on sensing and expert rules. UC E-1 aims at magnetic PD sensing to overcome limitations of existing galvanic and high frequency current transformers (HFCT) for, e.g. non-intrusive PD detection in underground cable joints remote from substations. IWO, TUD and IUNET studied PD signal paths and defined system requirements.

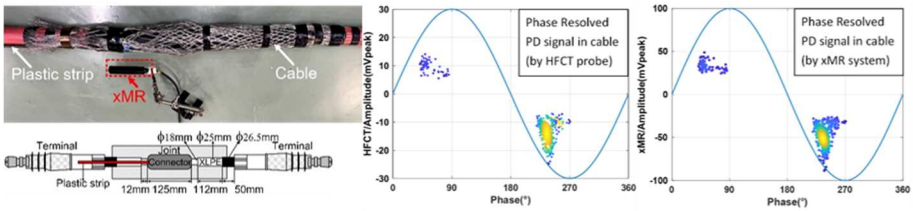

Fig. 9.1: MV cable with PD source in joint used for testing PD sensing systems.

Sensor families were explored for high sensitivity, such as: Superconductive Quantum Interference Devices (SQUIDs) and Magneto Resistance meter (MR) types. IWO, TUD, HAN and Sensitec found a GMR (Giant MR) sensor to be adequate for transients. For PD, an xMR sensor (Nivio TDK) for medical applications, appeared most promising. Its sensitivity approaches SQUIDs, but the xMR has the decisive advantage of working at room instead of cryogenic temperatures. For PD sensing, though, its 10 kHz range required a considerable extension to ≥10 MHz. The TU Delft HV Lab with IWO developed an HF signal processing unit for xMR.

This system was tested to successfully detect PD signals comparable to an HFCT sensor, but non-invasive. The TU Delft HV Lab demonstrated its capabilities for a realistic defect in an actual power cable section as well as for a defect in an actual HV Gas Insulated System set-up. The system is to be elaborated further for field tests.

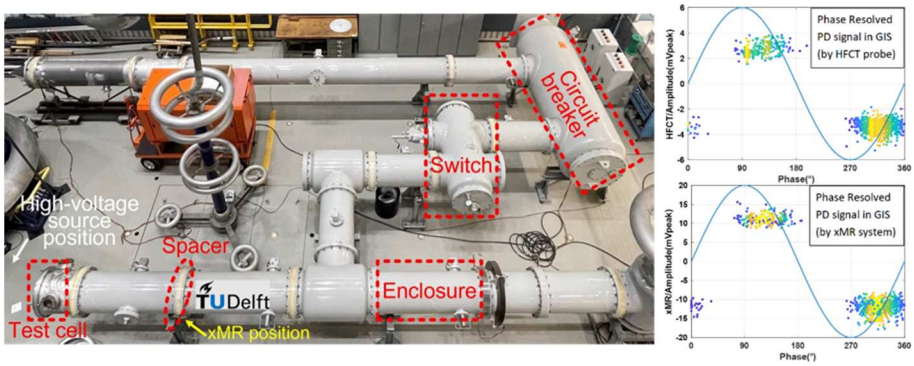

Fig. 9.2: The xMR was able to meet HFCT performance also for a GIS system.

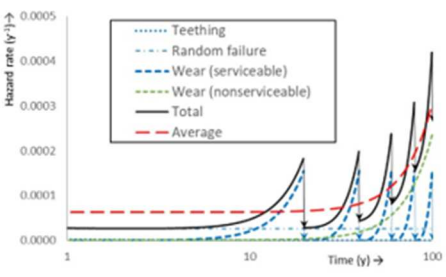

Fig. 9.3: Various types of failure mechanisms for which performance of prognostics is studied.

SELECTED TECHNICAL INNOVATIONS

#10. Material development and testing for component protection under harsh conditions (E-3)

(Use case example, Objectives no. 3, 5)

Encapsulation material is used to protect electronic components from aggressive media. However, these materials often react under environmental conditions in a function-impairing manner. The knowledge of the aging- and interaction mechanisms is essential for predicting their protective function and the service life of the corresponding electronic assembly. State of the art formulations for protective coatings of electronic devices are equipped with pigments or fillers that do not provide additional protection via a barrier functionality. Furthermore, the corrosion protection of commercially available mold materials is currently only given by standard polymers and fillers, which have remarkable permeation rates for humidity and harmful gases.

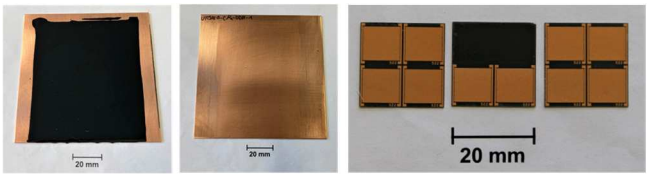

Fig. 10.1: Samples of epoxy-novolac with active corrosion inhibitors (left) and barrier coating with modified barrier pigments on copper substrates (center and right).

Fig. 10.2: Sample holder of UBremen with silicon gel mold material (left); device after ageing without (center) and with (right) scavenger.

Within the iRel40 project Fraunhofer IFAM is developing new coating and molding materials to address these weak points and prolong the lifetime of the protected electronic components through the targeted use of barrier pigments, active corrosion inhibitors and scavenger materials. The goal is to achieve an optimal combination of these materials to obtain the best protection for the electronic devices. Therefore, the adhesion of the materials is tested and optimized for various structures. To achieve optimal interlayer adhesion and compatibility, plasma interlayers and/or adhesion promoters are used.

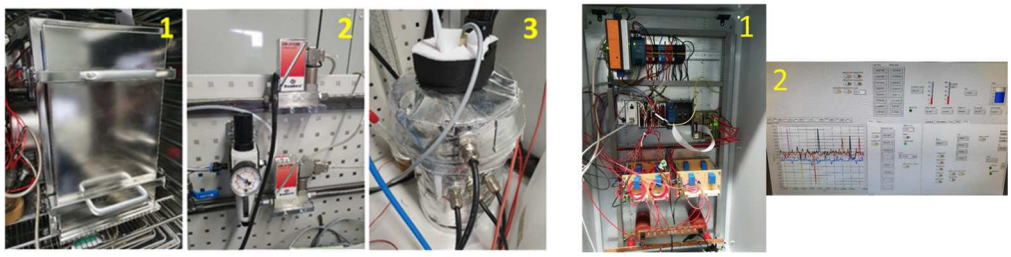

Fig. 10.3: Weathering setup at UBremen. Left: Corrosion chamber (1), mass-flow-controllers (2) and humidity system (3). Right: High voltage data acquisition system (1) and LabVIEW interface (2).

The testing of power semiconductor devices under high temperature, high humidity, a defined corrosive gas concentration and high voltage is the task of UBremen in the use case. The testing of power modules under high humidity showed a strong acceleration of aging due to high voltage bias. The method was extended to corrosive gas testing in the iRel40 project and offers the possibility to assess embedded semiconductor modules for their stability under harsh conditions.

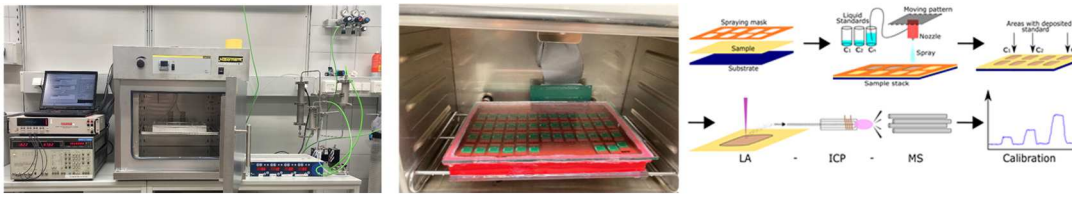

Fig. 10.4: Most recent weathering setup at TU Wien/KAI (left) with weathering cell (center). Schematic procedure of standard preparation and measurement for LA-ICP-MS calibration enabling quantitative analysis.

#11. Investigation for predictive reliability of potted LED drivers based on a simulation-based approach (DI-3)

(Use case example, Objectives no. 2, 3, 5)

Potting on LED drivers could bring a lot of benefits in outdoor lighting systems, such as mitigating the heat concentration, increasing the resistance to shock and vibration, and such on. However, due to the mismatching properties between potting compounds and those electronic devices, high thermo-mechanical stress could be introduced to the devices and solder interconnects during power cycling. To improve lifetime of LED drivers it is essential to get a deeper understanding of the behavior of the potting material and its influence to the electronic device.

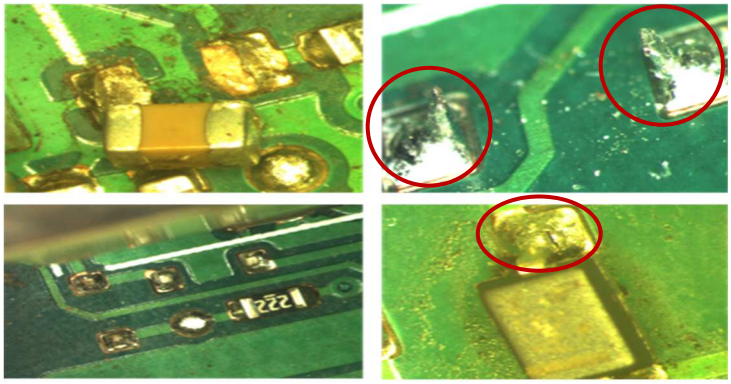

Fig. 11.1: Typical failures due to high accelerated power cycle tests, source: Signify.

The viscoelastic properties are quite important as the ability to relax intrinsic stresses and the coefficient of thermal expansion are quite temperature dependent. A special challenge was the glass transition temperature of the potting material, which is comparable low and lies near room temperature.

The general goal for the described approach is deriving best practice guidelines for material preselection and/or design generation to improve the reliability for similar assemblies in future. According to the specific test strategy the thermal conditions like temperature swing and cycle duration can be quite different which influences the thermo-mechanical reliability (see Fig. 11.2). To respects these facts already during the early design phase, a parametric FE simulation model for the LED driver demonstrator assembly was generated. It consists of a resistor and diode mounted on a PCB (Fig. 11.3). As industrial standard components were used, no valid CAD data was available for the inner structure of the diode. To get sufficient information Computer Tomography (CT) scans and cross-sections were used. A DoE study is now conducted to identify most influential parameters and relationship for the accumulated creep strain in the solder connections (Fig. 11.4).

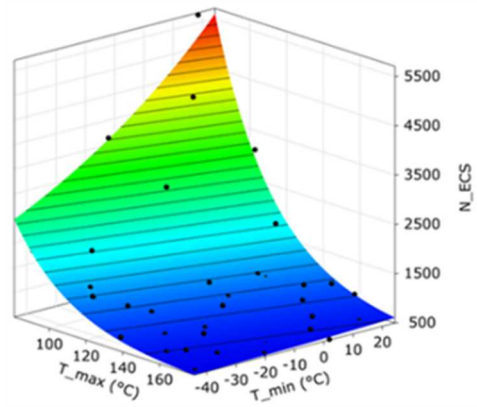

Fig. 11.2: Relationship of maximum cycle number and temperature swing obtained by a DoE study, source: FhG ENAS.

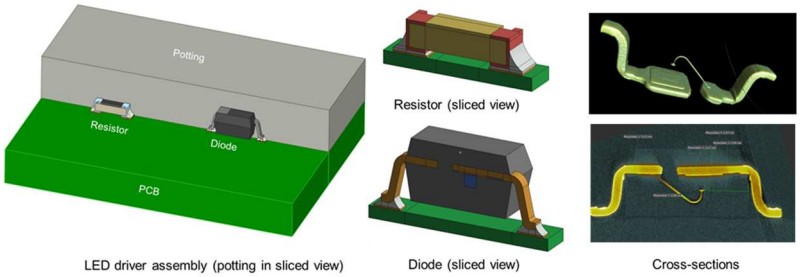

Fig. 11.3: Generated simulation model for the LED driver assembly (left, middle), obtained by CAD , CT scans and cross-sections (right), source: FhG ENAS.

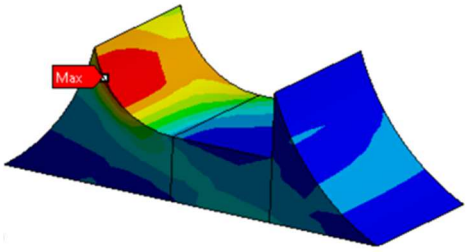

Fig. 11.4: Accumulated creep strain in the diode solder connection, source: FhG ENAS.

SUMMARY OF SELECTED DELIVERABLE

ML/AI applied (Deliverable D2.8)

This deliverable D2.8 reports the main advances performed on the implementation of AI/ML algorithms during the iRel40 project. The first aim of this task is to combine the pipelines for data processing with the developed AI/ML models and implement them as unified frameworks for applying AI/ML in reliability. The second aim is to optimize these frameworks so that they better align with the real world conditions and make them usable for holistic testing assessment in WP5. Data-driven models implemented in this task are used for (1) detecting indications to potential early fails and possibly to unwanted events within the development and fabrication phases of new electronic components and systems along its entire value chain, as well as (2) detecting early signs of degradation during the service of the systems, which will ultimately lead to wear-out failures.

The models being implemented under this task stem purely from the data and are based on AI routines using techniques like deep-learning neural networks, decision trees, probabilistic models, and others. The implemented routines shall allow streaming of large amounts of data, identifying the relevant patterns automatically. The developed AI algorithms will recognize even slight modifications in the patterns of the streamed data (such as wafer maps, process control charts, and feedback data from the field), classify these signatures, and determine whether they indicate a potential early failure or a wear-out effect, respectively.

The models implemented in this task are being hybridized with physics of failure models in Objective 2.4. This incorporates expert knowledge directly into the models making their training less dependent on data. This is advantageous because data gathered for real industrial problems can be of low quantity and not exhaustive given all failure phenomena. Data-driven models are fully dependent on data and its quality, however, they are essential constituents of hybrid, physics-informed models that have greater generalization abilities than purely data-driven ones.

Use cases considered in this deliverable are very diverse with respect to the objective and the properties of the available data. Based on these factors various machine learning and statistical methods were implemented and tailored to the use case aim and the underlying data characteristics. To successfully face their current reliability issues specialized techniques were perfected for dealing with use case specific obstacles such as low data quantity, class imbalance, heterogeneous data, intercorrelations in the data and so on. In this document, for each use case, the implementation of suitable data-driven modelling techniques is described.

Reliability concerns are quite different for different use cases as well as the physics behind it. However, methods reported here put them on a similar standpoint given the universality of AI/ML/statistical methods used. This deliverable report shows that no single method is ideal and the efficiency of data-driven techniques vary greatly depending on the problem at hand. Based on the work reported here we can extract guidelines for dealing with different reliability problems, depending on the type of reliability concern and data properties. We can also see that real-world data connected to reliability usually has some troublesome properties which makes data-driven modelling mode difficult than expected. To deal with them, partners developed and applied several techniques and model customizations, that were useful in different use cases and represent an important example of synergy among use cases and advance in improvement of know-how in data-driven modelling when used in reliability.

Data is of paramount importance in data-driven modelling, the effects of these delays are largely not noticeable. Even in cases where data is currently still quite limited the framework for data-driven modelling was prepared and tested on surrogate data that is in some manner analogous to the expected full data set.

SUMMARY OF SELECTED DELIVERABLE

Report on physics of failure digital twin concepts for fabrication and service (Deliverable D2.10)

This deliverable D2.10 reports innovations achieved in physics of failure digital twin concepts for fabrication and service. In the modern development of electronic components and systems (ECS), digital twins (DT) play a crucial role to drive innovation and improve performances. Nowadays, complex engineering equipment is used during the product development and the lifecycle of any product or process. Digital Twins replicate the physical object or process by using real word data to create virtual models that can predict the performance and thus enhance the reliability.

The main objective of this deliverable is to report on the development of DT concepts based on physics of failure. Currently, in the ECS industry, due to the growing number of functionalities, several chips, components, sensors, modules etc. need to be integrated. However, such integration makes the system very complex and prone to different failure modes. To cope with such complexity, the next generation DT needs to be robust, flexible and adaptive. In this deliverable, several digital twin concepts focusing on wide range of applications are described. To address the complex technical challenges, the described DTs use various modern concepts and tools such as Artificial Intelligence, Virtual Reality, Finite Element Models and many more for modelling the virtual behavior of novel products such as VCSELs, a current sensor device etc. The developed digital twins also touch several reliability concerns and proposes new ways incorporating new physics of failure models. The application area span across automotive, packaging industry, several electronic modules and medical sectors.

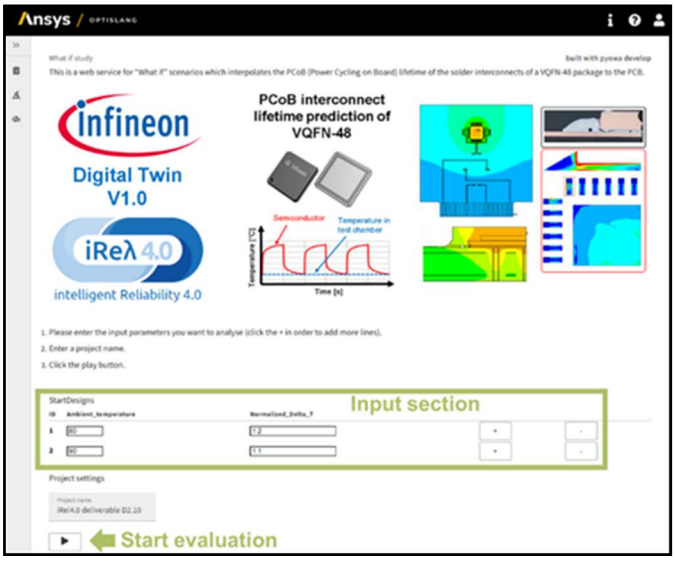

Fig. 12.1: View of the web front-end of digital twin version 1.0 of Infineon.

Overall, the 11 UCs and IP address the objective 2 and objective 3 of the iRel40 project and propose novel approaches to develop next-generation digital twins.

Fig. 12.1 shows an example of Infineon, where the web front-end of the digital twin is shown. The interface allows the users to define in the input section, the ambient temperature and the normalized Delta-T DT generated by the dissipated power for the respective cooling condition. By pushing the "play" button, the computation of the digital twin is initiated. The advantage of the digital twin provided as a web service compared to FEM-based simulation is, that its computation takes only seconds compared to hours of FEM simulation. This clearly suits better the needs of reliability engineers.

SUMMARY OF SELECTED DELIVERABLE

Physics of Failure – Compact modelling strategies (Deliverable D2.12)

This deliverable D2.12 gives a general introduction to the concept of compact modelling and related concepts in the iRel40 project. Due to the fact that the term "compact modelling" covers different modelling approaches, comprising physically based, empirical as well as data based approaches, the presented work represents several compact modelling concepts. In the context of Finite Element Analysis (FEA), compact modelling involves the creation of simplified models that capture the key aspects of the physical system, while neglecting less significant details. These compact models can then be used to approximate the FEA results, providing a faster and more efficient prediction. For example, compact models can be used to reduce the number of degrees of freedom required for a simulation, by reducing the complexity of the finite element model. This can reduce computational cost of the simulation, while maintaining a high level of accuracy. In a reliability context, compact models are commonly used to approximate the thermal and mechanical response of systems to an external load in a computationally efficient way, as shown in Fig. 13.1.

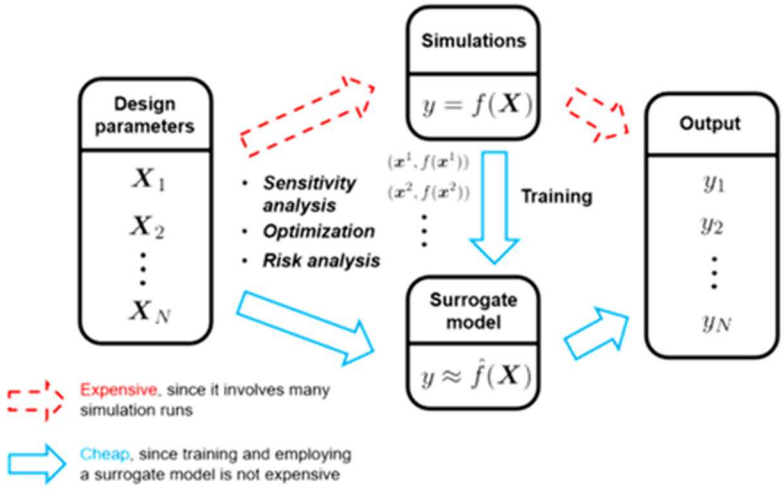

Fig. 13.1: Basic concept of compact modelling: Approximation of a heavy weight simulation model (FEA, etc.) by a numerically cheap model derived from the numerically expensive model.

As an example for a compact modelling concept with a physical background, an improved method for lumped thermal modelling of ECS, based on the formal analogy of the thermal laws and electrical Ohm's law is developed. It is shown why the lateral heat transfer for PCBs need to be considered in the overall heat transfer models.

Furthermore, a different type of compact model that uses the idea of a super element is introduced. The software package ABAQUS (www.simulia.com) allows to define so called "substructures" which correspond to super elements in FEA.

Another focus of the work has been put on establishing data-based models that are derived from FEA training sets. It is shown how a virtual DoE can generate stochastic results.

Additionally, the feasibility and potential of the application of compact models for the prediction of the behavior of ECS under several load profiles for different application cases was shown.

Especially, the use of compact modelling strategies for virtual DoEs during the development, allowing early and fast understanding of the system response e.g. by a response surface covering the whole design area, opens new possibilities with regard to design for reliability and thus supports perfectly the targets and objectives of iRel40.

SUMMARY OF SELECTED DELIVERABLE

Combination of PoF and data-driven models (Deliverable D2.13)

This deliverable D2.13 is dedicated to identifying and analysing possible hybridization concepts for the development of the prognostics & health management (PHM) strategy. In short, it covers the combination of data-driven and physics-based models to enable the implementation of PHM solutions to the various use cases and industrial pilots within the project. This deliverable describes the hybrid modelling work carried out in 12 out of the 34 use cases that are involved in this task. For each use case three main topics are covered:

- Physics-based models (connects to O2.3)
- Data-driven models (connects to O2.2)
- Hybrid model (connects to the rest of O2.4)

The results demonstrate, that due to the variability in the different use cases, it is difficult to fit a framework of hybrid modelling that can accommodate all these diverse needs. Each use case comes with its own set of challenges and conditions. They are quite different from each other. In the last part of the project work is ongoing to find and develop commonalities and overarching principles for hybrid modelling in ECS.

Fig. 14.1 shows an example of a hybrid model developed in Industrial Pilot 3 as part of D2.13, enabling component stress-strength analysis in induction cooktops by combing physics-of-degradation with data driven models.

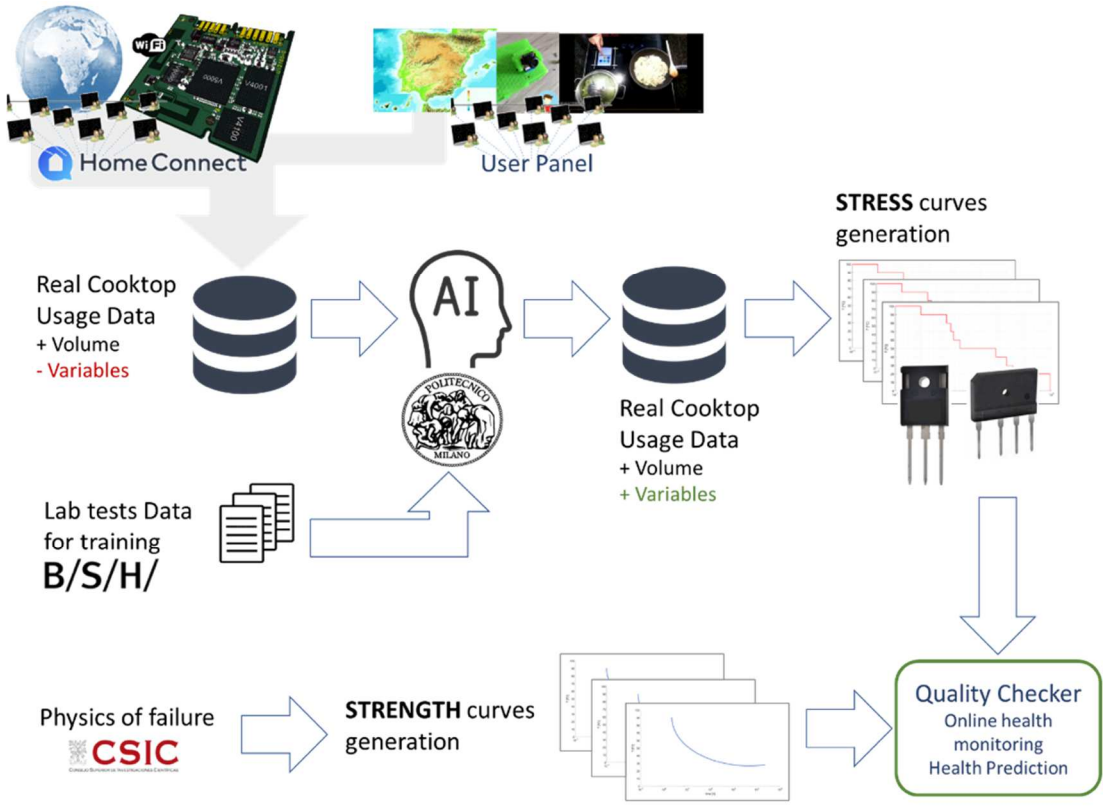

Fig. 14.1. Taking the stress and strength data into account, hybridising PoF and data driven models, the sum of damage produced by a specific user can be calculated at design element level (from IP-3).

DISSEMINATION

Scientific results published as book chapters, conference contributions or journals papers

Books

3 book chapters in "Reliability of Organic Compounds in Microelectronics and Optoelectronics", ed. W. D. van Driel and M. Y. Mehr, Springer, 2022. ISBN 978-3-030-81575-2, DOI: 10.1007/978-3-030-81576-9:

- "Reliability and failures in solid state lighting systems", pp. 211-240
- "Outlook: From physics of failure to physics of degradation", pp. 535-538
- "Reliability and Degradation of Power Electronic Materials", pp. 449-478

Conference Contributions

19 published journal papers and close to 100 presented and planned conference contributions and presentations for "31st European Safety and Reliability Conference (ESREL)", "IEEE 8th Workshop on Wide Bandgap Power Devices and Applications (WIPDA)", "2021 IEEE International Electron Device Meeting (IEDM 2021)", "2021 IEEE International Integrated Reliability Workshop (IIRW)", "IEEE International Conference on Connected Vehicles and Expo 2022 (ICCVE2022)", and International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE 2023) and others. The list of published conference contributions is available on the project webpage *www.iRel40.eu*, section outcome.

Published journal articles

1. Olschewski, T., "*Fast Accurate Defect Detection in Wafer Fabrication"*, arXiv preprint, arXiv:2108.11757 (2021).
2. Millesimo, et al., "*High-Temperature Time-Dependent Gate Breakdown of p-GaN HEMTs*", IEEE Trans. on Electron Devices 68, no. 11 (2021): 5701-5706.
3. Tallarico, et al., *"TCAD Modeling of the Dynamic V TH Hysteresis Under Fast Sweeping Characterization in p - GaN Gate HEMTs*", IEEE Trans. on Electron Devices 69, no. 2 (2021): 507-513,
4. Olschewski, T., "*Defect Detection on Semiconductor Wafers by Distribution Analysis*", arXiv pre print, arXiv:2111.03727 (2021).
5. Safari, L. et al., "*Towards Realization of a Low-Voltage Class-AB VCII with High Current Drive Capability*", Electronics 10, no. 18 (2021): 2303.
6. Van Driel, W. D., et al., "*Reliability of LED-based systems*", Microelectronics Reliability 129 (2022): 114477.
7. Meneghini, M., et al., "*GaN-based power devices: Physics, reliability, and perspectives"*, J. Appl. Phys. 130, no. 18 (2021).
8. Bonet, F., et al., "*Carrier Concentration Analysis in 1.2 kV SiC Schottky Diodes under Current Crowding"*, IEEE Electron. Dev. Letters 43, no. 6 (2022).
9. De la Rosa, Francisco López, et al., "*Geometric transformation-based data augmentation on defect classification of segmented images of semiconductor materials using a ResNet50 convolutional neural network"*, Expert Systems with Applications (2022): 117731.

Published journal articles — continued

10. Hagara, Miroslav, et al., "*Modified algorithm of unimodal thresholding for FPGA implementation*", Microprocessors and Microsystems 94 (2022): 104669.
11. López de la Rosa, Francisco, et al., "*A review on machine and deep learning for semiconductor defect classification in scanning electron microscope images*", Applied Sciences 11.20 (2021): 9508.
12. Modolo, N., et al., "*Compact Modeling of Nonideal Trapping/Detrapping Processes in GaN Power Devices*", IEEE Transactions on Electron Devices 69.8 (2022): 4432-4437.
13. De la Rosa, Francisco López, et al., "*A deep residual neural network for semiconductor defect classification in imbalanced scanning electron microscope datasets*", Applied Soft Computing (2022): 109743.
14. Millesimo, M., et al., '*The Role of Frequency and Duty Cycle on the Gate Reliability of P-GaN HEMTs*", IEEE Electron Device Letters, vol. 43, no. 11, (2022): 1846–49.
15. Kemeny, Martin, et al., "*Comprehensive Degradation Analysis of NCA Li-Ion Batteries via Methods of Electrochemical Characterisation for Various Stress-Inducing Scenarios*", Batteries, vol. 9, no. 1, (2023): 33.
16. Chen, Yun, et al., "*Giant Magneto-Resistive (GMR) Sensors for Non-Contacting Partial Discharge Detection*", IEEE Transactions on Instrumentation and Measurement, vol. 72, (2023): 1–11.
17. Willner, Jakob, et al., "*A Versatile Approach for the Preparation of Matrix-Matched Standards for LA-ICP-MS Analysis – Standard Addition by the Spraying of Liquid Standards*", Talanta, vol. 256, (2023): 124305.
18. Mo, Jiarui, et al., "*A Highly Linear Temperature Sensor Operating up to 600°C in a 4H-SiC CMOS Technology*", IEEE Electron Device Letters, (2023): 1–1.
19. Mehra, Sumiran, et al., "*An Empirical Evaluation of Enhanced Performance Softmax Function in Deep Learning*", IEEE Access, vol. 11, (2023): 34912–24.

iRel40 Book: it's coming!

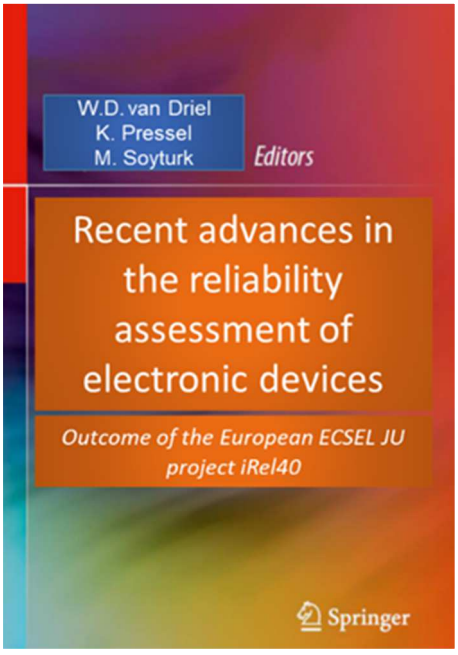

Fig. 15.1. iRel40 book cover.

We started almost a year ago to announce our idea for a book, entitled: "*Recent advances in the reliability assessment of electronic devices*". Quite soon we found Springer to agree on hosting this book. After a first call for chapters, we realized 20 different chapters in the areas i) Multi-scale & multi-physics simulations for physics-of-degradation, ii) AI based control systems in advanced production, iii) Smart sensing and big data analysis, iv) Reliable Materials, Reliability Testing and Diagnostics, v) Prognostic and health management / digital twin / condition monitoring and vi) Design. Per today, 10 out of 20 chapters have arrived in good order, accounting for 245 pages of new insights in the reliability domain. The other half of the chapters are expected to arrive in due time, not later than 1st of September.

Willem, Klaus & Mujdat.

GENERAL ASSEMBLY MEETING

Crete, May 9-12, 2023

The third face-to-face General Assembly meeting of the ECSEL JU project iRel40 took place from Tuesday, May 9th to Friday, May 12th, 2023, in Rethymno, Crete. Close to 90 participants of the iRel40 consortium joined, which consists of 75 partners from 13 countries. They discussed the project progress and planned the next steps to finalize the project successfully until October 2023.

Fig. 16.1: iRel40 team during the third General Assembly meeting in Crete.

During the meeting, a detailed status summary of the project was provided by the coordinator and work packages leaders.

Within the Crete meeting, several workshops were organized by workpackage leaders focusing on different aspects of reliability for electronic components and systems. WP2 organized two workshops on Hybrid Modelling and Physical Health Management (PHM). These workshops focused on the impact of predictive models, fault detection and diagnosis, prognostics, and health management on reliability improvement of electronics components and systems (ECS). Two final deliverables are presently in progress on these topics for the end of the project. Another workshop organized by WP5 focused on holistic testing and identification of key performance indicators (KPI).

Fig. 16.2: Participants during the presentation of the project status.

WP4 presented the status on intelligent manufacturing and testing. WP3 presented the status on material simulation and compact modelling. WP3 especially drives the test vehicle catalogue, which includes work on single bricks to improve reliability.

A detailed part of the meeting was the presentation of the status of the use cases. Meanwhile important reliability results are available, which now need to be implemented into a bigger picture. All the 34 use cases were presented in a highlight presentation and an accompanied poster.

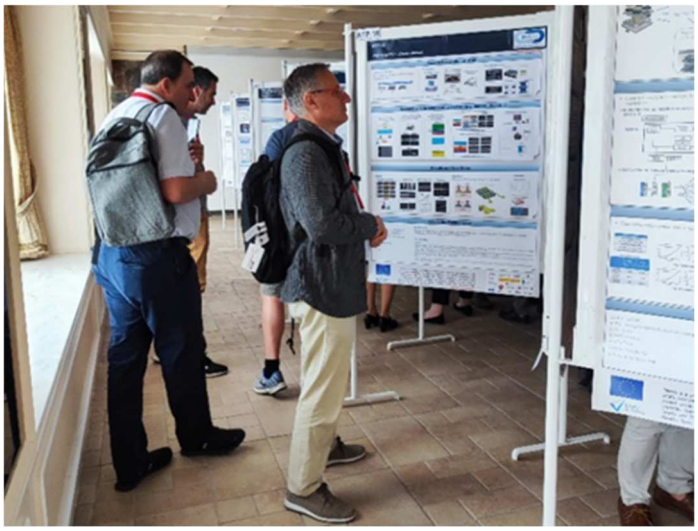

Fig. 16.3: Participants during the use case poster session.

For strengthening important research of PhD students an additional poster session has been organized. 12 highlights were presented either related to use cases or test vehicles. The use case and PhD poster presentations organized by WP6 during the iRel40 meeting fostered conversations between the different work packages and engaged PhD students into the topics related with all the aspects of reliability.

To recognize best works awards to the best use case and best student poster were granted. The award for the best use case poster was granted to Julia Zündel from AT&S on "*Application of a design limits based, predictive design approach for the design of a reliable M2X module*. The best student poster award was granted to Joshua Lommes from Fraunhofer IFAM for his presentation on "*Organic modification of layered silicates as barrier pigments in coating systems to protect electrical devices"*.

The project is in the final stage and many results are already achieved. A magnitude of publications are in progress including a book on iRel40 outcome. Close to 100 publications based on journal and conference articles were meanwhile published. These numbers are continuously increasing due to a high number of planned and submitted papers.

Fig. 16.4: The awards ceremony with awards of the best use case poster granted to Julia Zündel from AT&S and best student poster granted to Joshua Lommes from Fraunhofer IFAM.

The Crete meetings allowed us to discuss the results in the final stage of the project and tuned the last actions towards a successful fulfillment of project goals. The project results have the potential to strengthen and development production along the value chain and support the sustainable success of investment in microelectronics in Europe through the improvements of the reliability of electronic systems. More information can be found at our website www.iRel40.eu.

iRel40 results presented during EuroSimE 2023

(EuroSimE 2023 April 16th - 19th 2023 at Graz, Austria)

The 24th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems took place in Graz, Austria, between 16th and 19th of April, 2023. More than 160 participants discussed their latest results on the topic and impact on reliability improvement. It was one of the best ever visited EuroSimE events (only Berlin in 2005 and Gent in 2014 had more participants). In 2023 the EuroSimE Technical Committee made substantial effort to bring an exciting face to face program together. This program finally included:

- 22 sessions comprising of oral and poster presentations (plus an excellent keynote session)
- 4 short courses given by distinguished speakers from industry and academia
- An additional IEEE Heterogeneous Integration Roadmap (HIR) session combined with IPCEI and iRel40 project results.

Extensive opportunities were offered for technical exchange between participants and exhibitors of computer simulation software and characterization equipment. Using sponsoring, the EuroSimE Committee was able to offer reduced fees for PhD students, pushing their share to 25% of the attendees: This allowed for knowledge exchange towards the next generation of engineers in the field of semiconductor reliability. The iRel40 project contributed with a significant amount of nine accepted contributions to the program. Three iRel40 contributions were presented during the interactive poster session:

- *"Influence of the quality of material models on warpage and lifetime prediction by finite element simulation"* by Julia Zündel et al. This was a contribution by iRel40 project partner AT&S Austria Technologie & Systemtechnik AG (Austria).

The contribution of Julia Zündel from AT&S received the **outstanding poster award** of the EuroSimE 2023 conference (see Fig. 17.1, right).

Fig. 17.1: During the poster session, two iRel40 poster contributions were presented: (left) members of the iRel40 team Bart Vandevelde (right, IMEC), Dag Andersson (middle, RISE) together with Markus Weninger (left, AT&S); (right) Julia Zündel (AT&S) received the Outstanding Poster award by the conference chair Willem van Driel (Signify).

- "*Evaluation of thermomechanical behavior of electronic devices through the use of a reduced order modelling approach"* by Markus Weninger et al. This was a cooperation of AT&S Austria Technologie & Systemtechnik AG (Austria), Polymer Competence Center Leoben GmbH (Austria), and Prime Aerostructures GmbH (Austria);
- "*Deformation analysis of QFN packages for validation of thermo-mechanical finite element simulations*" by Chinmay Nawghane, Bart Vandevelde (all IMEC), Thomas Moncond'huy, Pierre Vernhes, Rodolfo Cruz (all Insidix).

Further five iRel40 papers were presented during EuroSimE 2023. These were:

- *"Ab-initio derived force field potential for accurate simulation of thermal transport in AlN"* by Simon Fernbach, Elke Kraker, Natalia Bedoya-Martinez (Material Center Leoben, Austria);
- "*Characterization and simulation of delamination on package-level considering sub-critical interfacial fracture-parameters under cyclic loading",* by Rudolf Kniely (*ams OSRAM Group),* Jens Heilmann (*Chemnitz University of Technology*), Fabian Huber (*ams OSRAM Group),* Bernhard Wunderle (*Chemnitz University of Technology, Fraunhofer ENAS);*
- "*Size Scaling of Brittle Strength using Multi-Mode Weibull Distribution, Infineon Technologies AG* by Sergey Ananiev, G.M. Reuther, N. Del Vecchio, P. Altieri-Weimar (Infineon Technologies AG);
- *"Strain Measurements and Thermo-Mechanical Simulation of SnAgCu vs. low melting point alloy (LMPAQ) solder joints",* by Bart Vandevelde (IMEC Belgium) et al.
- Micro-cantilever Bending Test of Sintered Cu nanoparticles for Power Electronic Devices by Leiming Du, Dong Hu, René Poelma, Willem van Driel, Kouchi Zhang (TU Delft, Signify, Nexperia).

An additional iRel40 project result was presented during the Heterogeneous Integration Roadmap (HIR) session. Klaus Pressel contributed with an iRel40 related presentation entitled "*Reliability along the Value Chain – from Chip to Board/System"* to this session. Since its 2021 version the HIR has an own chapter on Reliability. Based on their roadmap discussions the HIR experts identified reliability as a major topic. To this chapter iRel40 members significantly contribute, e.g. Bosch, Signify, Infineon, Fraunhofer. The HIR session was also combined with results from the iRel40 and the IPCEI ME project. The presentations demonstrated the importance of the link between the ECSEL JU project iRel40 and the IPCEI ME project in respect to reliability and advanced manufacturing.

Fig. 17.*2: Klaus Pressel of Infineon presenting the iRel40 project and importance of reliability along the value chain during the Heterogeneous Integration Roadmap* (HIR) *session.*

In summary, the EuroSimE conference, which brings together important players from industry and research institutes, demonstrated also in 2023 to be an important conference which covers key aspects of the iRel40 project. The conference is an excellent hub sharing iRel40 results and driving methods on reliability improvement forward. Also during the next EuroSimE conference scheduled in April 2024 at Catania Italy, iRel40 project partners will have significant contributions to a number of sessions.

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